Claims

1. A dual gate oxide high-voltage semiconductor device, comprising:

a buried oxide layer formed over a semiconductor substrate;

a silicon layer formed over the buried oxide layer;

a top oxide layer formed over the silicon layer;

a first gate oxide formed over the silicon layer adjacent the top oxide layer; and

a second gate oxide formed over a portion of the first gate oxide.

2. The device of claim 1, wherein the silicon layer comprises a source region, a body region, and a drift region.

3. The device of claim 2, wherein the first gate oxide is formed over the drift region, the body region, and the source region.

4. The device of claim 2, wherein the second gate oxide is formed over the first gate oxide between the top oxide layer and the body region.

5. The device of claim 1, further comprising a field plate formed over the top oxide layer, the first gate oxide, and the second gate oxide.

6. The device of claim 1, wherein the first gate oxide has a thickness in a range of approximately 300-600A, and wherein the second gate oxide has a thickness in a range of approximately 900-1200A.

7. The device of claim 1, wherein the first gate oxide has a length of approximately 3-4μm, and wherein the second gate oxide has a length of approximately 1-2μm.

8. A dual gate oxide high-voltage semiconductor device, comprising:

a buried oxide layer formed over a semiconductor substrate;

a silicon layer formed over the buried oxide layer, wherein the silicon layer comprises a source region, a body region, and a drift region;

a top oxide layer formed over the silicon layer;

a first gate oxide formed over the silicon layer adjacent the top oxide layer; and

a second gate oxide formed over a portion of the first gate oxide between the top oxide layer and the body region.

9. The device of claim 8, further comprising a field plate formed over the top oxide layer, the first gate oxide and the second gate oxide.

10. The device of claim 8, wherein the first gate oxide has a thickness in a range of approximately 300-600A, and wherein the second gate oxide has a thickness in a range of approximately 900-1200A.

11. The device of claim 8, wherein the first gate oxide has a length of approximately 3-4μm, and wherein the second gate oxide has a length of approximately 1-2μm.

12. The device of claim 8, wherein a thickness of approximately 1200A for the second gate oxide results in an increase from approximately $1e^{12}cm^{-2}$ to approximately $2e^{12}cm^{-2}$ for a maximum allowable charge, and wherein a decrease of approximately 30% for a specific-on-resistance, of the device.

13. A method for forming a dual gate oxide high-voltage semiconductor device, comprising:

forming a buried oxide layer over a semiconductor substrate;

forming a silicon layer over the buried oxide layer;

forming a top oxide layer over the silicon layer;

forming a first gate oxide adjacent the top oxide layer over the silicon layer; and

forming a second gate oxide over the first gate oxide.

14. The method of claim 13, wherein forming the first gate oxide, and forming the second gate oxide comprises:

growing the first gate oxide adjacent the top oxide layer over the silicon layer;

applying a mask over the first gate oxide; and

growing the second gate oxide over a portion of the first gate oxide.

15. The method of claim 13, wherein forming the silicon layer comprises forming a silicon layer having a source region, a body region, and a drift region over the buried oxide layer.

16. The method of claim 15, wherein forming the first gate oxide comprises forming a first gate oxide over the drift region, the body region, and the source region.

17. The method of claim 15, wherein forming the second gate oxide comprises forming a second gate oxide over the first gate oxide between the top oxide layer and the body region.

18. The method of claim 13, further comprising:

increasing a maximum allowable charge of the device from approximately $1e^{12}cm^{-2}$ to approximately $2e^{12}cm^{-2}$; and

decreasing a specific-on-resistance of the device by approximately 30%.

19. The method of claim 13, wherein forming the first gate oxide and forming the second gate oxide comprises:

forming a first gate oxide having a thickness in a range of approximately 300-600A adjacent the top oxide layer over the silicon layer; and

forming a second gate oxide having a thickness in a range of approximately 900-1200A over the first gate oxide.

20. The method of claim 13, further comprising forming a field plate over the top oxide layer, the first gate oxide, and the second gate oxide.